IN THE SPECIFICATION:

Please amend the paragraphs in the specification as follows:

[0058] In the photosensitive region 10, pixels 11_{mn} are two dimensionally arranged in ~~M rows and N columns~~ N rows and M columns. One pixel is constituted by a photosensitive portion 12_{mn} (first photosensitive portion) and a photosensitive portion 13_{mn} (second photosensitive portion), which output respective currents corresponding to intensities of light incident thereon, are arranged adjacent to each other within a single plane. As a consequence, the photosensitive portions 12_{mn} and 13_{mn} are arranged within the same plane in a state two-dimensionally mingling with each other.

[0083] Reference will be made to Fig. 9 again. The first maximum value detecting circuit 140 detects the maximum value of respective voltages outputted from the first S/H circuits 130. As shown in Fig. 13, the first maximum value detecting circuit 140 comprises NMOS transistors T_1 to T_M, resistors ~~R_1 to R_3~~ R_1, R_2, and R_{dd}, and a differential amplifier A_4. The source terminal of each transistor T_m is grounded. The drain terminal of each transistor T_m is connected to power supply voltage V_{dd} by way of a resistor R_{dd}, and is connected to the inverting input terminal of the differential amplifier A_4 by way of a resistor R_1. The gate terminal of each transistor T_m is connected to the output terminal of its corresponding first S/H circuit 130, so as to receive the voltage outputted from the first S/H circuit 130. A resistor R_2 is disposed between the inverting input terminal and output terminal of the differential amplifier A_4, whereas the non-inverting input terminal of the differential amplifier A_4 is grounded. In the first maximum value detecting circuit 140, voltages outputted from the first S/H circuits 130 are fed into the gate terminals of their corresponding transistors T_m, and a potential corresponding to the maximum value of the

voltages appears at the drain terminals of the transistors T_m. The potential of the drain terminals is amplified by the differential amplifier A_4 with an amplification factor corresponding to the ratio between respective ohmic values of the resistors R_1 and R_2, whereby the value of thus amplified voltage is outputted as the maximum voltage V_{max1} from the output terminal to the first level shift circuit 170.

[0089] The first integrating circuits 210 are provided so as to correspond to the other group of photosensitive portions 13_{mn} (N rows of photosensitive portions, constituted by the other second conduction type semiconductor regions 42, lengthily extending in the second direction) electrically connected to each other in the plurality of pixels 11_{11} to 11_{M1}, 11_{12} to 11_{M2}, ..., 11_{1N} to 11_{MN} arranged in the second direction, and convert corresponding electric currents from the other photosensitive portion group 13_{mn} into voltages and output the voltages. Each second integrating circuit 210 has a configuration equivalent to that of the first integrating circuit 110 shown in Fig. 11, such that an amplifier, a capacitor, and a switch are connected in parallel between input and output terminals. The switch of the second integrating circuit 210 opens and closes according to Reset signal outputted from the second timing control circuit 220. The second timing control circuit [[120]] 220 outputs the Reset signal for controlling the opening and closing of the switch of the second integrating circuit 210, and Hold signal for controlling the opening and closing of switches of second S/H circuits 230 which will be explained later.

[0095] Thus, voltages V_{out} corresponding to the electric charges (electric currents) accumulated in the other photosensitive portion 13_{mn} group electrically connected together in a plurality of pixels 11_{11} to 11_{M1}, 11_{12} to 11_{M2}, ..., 11_{1N} to 11_{MN} arranged in the [[first]] second direction are

sequentially outputted as time series data per the other photosensitive portion 13_{mn} group corresponding thereto from the second S/H circuits 230 (second integrating circuits 210) to the second level shift circuit 270 as shown in Fig. 19 as well. This time series data indicates a luminous profile (analog data) in the first direction.

[0117] The second inverting circuits 290 are disposed downstream their corresponding second S/H circuits 230, invert the respective voltages outputted from the second S/H circuits 230, and output the inverted voltages, which are fed into the second maximum value detecting circuit 240 and the second switches 260. As a consequence, the second maximum value detecting circuit 240 functions as a minimum value detecting circuit for detecting the minimum value of respective voltages outputted from the second S/H circuits [[130]] 230. In the second A/D converter circuit 280, the range from the maximum value (V_{max2}) detected by the second maximum value detecting circuit 240 to a value smaller than the maximum value (V_{max2}) by a predetermined value (V_{shift2}), i.e., the range from the minimum value of respective voltages outputted from the second S/H circuits 230 (second integrating circuits 210) to a value greater than the minimum value by a predetermined value (V_{shift2}), is set as an A/D conversion range.